

(19)日本国特許庁 (JP)

(12) 公開特許公報 (A)

(11)特許出願公開番号

特開平5-55278

(43)公開日 平成5年(1993)3月5日

(51)Int.Cl. <sup>a</sup>	識別記号	序内整理番号	F I	技術表示箇所
H 01 L 21/56	E	8617-4M		
21/304	3 2 1	B 8831-4M		
21/78	L	8617-4M		
		9168-4M	H 01 L 21/ 92	B
		7352-4M	23/ 12	L

審査請求 未請求 請求項の数4(全6頁) 最終頁に続く

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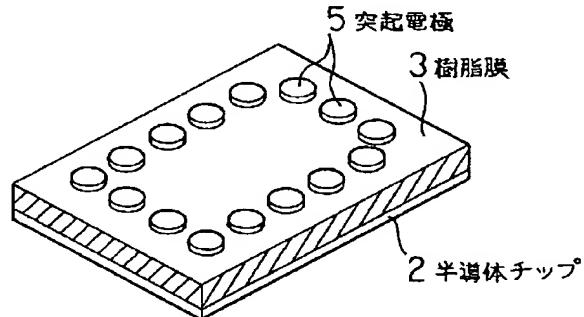
(54)【発明の名称】 半導体装置

(57)【要約】

【目的】半導体チップそのものの厚みを半導体ウェハの大きさによらず薄くさせながら、製造工程における半導体チップの取り扱い作業性を向上させ、かつ、小型、薄型の半導体装置を得る。

【構成】樹脂膜3を保護強化板としながら半導体ウェハ1を薄くし、かつ、半導体チップ2上の樹脂膜3から突起電極5を突出させて外部接続端子とし、樹脂膜3の大きさを半導体チップ2と同一になるように切断する。

【効果】高信頼性で取り扱い容易な、小型、薄型の半導体装置が得られる。



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## 【特許請求の範囲】

【請求項1】 半導体チップの側面および下面が露出し、前記半導体チップ上面にこれとほぼ同一の大きさを有する樹脂部が形成され、前記樹脂部の上面から突起電極が突設されていることを特徴とする半導体装置。

【請求項2】 前記樹脂部の最表面の主部に絶縁保護強化膜が形成されていることを特徴とする特許請求項1に記載の半導体装置。

【請求項3】 前記突起電極が埋設された樹脂部を保護強化板としながら半導体ウエハ裏面部を除去させたことを特徴とする特許請求項1に記載の半導体装置の製造方法。

【請求項4】 前記樹脂部から突起電極先端部および半導体ウエハの切断領域を露出させた後に、樹脂部最表面および切断領域表面に絶縁保護強化膜を形成し、切断領域を切断することを特徴とする特許請求項1に記載の半導体装置の製造方法。

## 【発明の詳細な説明】

## 【0001】

【産業上の利用分野】 本発明は半導体チップのパッド電極膜上に形成された突起電極先端部を外部接続端子とつなぐ半導体装置に関する。

## 【0002】

【従来の技術】 一般にパターン形成が完了した半導体ウエハは裏面研削法を用いて所定の厚みに研削される。この裏面研削法は、保護フィルムとなる塩化ビニールなどを基材とする軟質性フィルムを半導体ウエハのパターン面に貼り付け、軟質フィルム上から半導体ウエハを均一に加圧して回転させながら、ダイヤモンド粒が樹脂中に練入された粒石により半導体ウエハ裏面を研削、除去するものである。

【0003】 そして研削された半導体ウエハのスクライブラインを切断して個々の半導体チップに分割し、半導体チップと外部端子リードとをボンディングワイヤあるいはTABリードなどを介して相互に電気的に接合させ、樹脂封止後に外部端子リードを加工形成させるというものが一般的な技術であった。

【0004】 また、半導体ウエハ上にAuバンプなどの突起電極を形成させるには、前記裏面研削法による半導体ウエハ裏面を研削し、除去する前もしくは後に、Crなどのバリア金属膜を形成して、Au電解メッキ法によりAuバンプを選択的に形成させていた。

## 【0005】

【発明が解決しようとする課題】 半導体装置は、コンピュータ、ワークステーション、パーソナルコンピュータ、ワードプロセッサ、携帯電話、小型携帯カムコーダなどのあらゆる機器に多量に搭載されている。近年、これらの機器の小型化、軽量化の進展は著しく、また、今後これらの機器の小型化、軽量化そして高性能化、高機能化はさらに進むことから、これらの機器に搭載される

半導体装置の小型化、薄形化、高信頼性化への要求は、半導体素子の高集積化、高機能化という要求と合わせて加速度的に増大していくものと予測される。しかしながら、半導体ウエハの大口径化の進展にともない従来の裏面研削法による半導体ウエハ厚の加工には、ハンドリング時もしくは研削時の半導体ウエハの破損防止という制約により厚みを薄くすることに限界が生じ、この結果、半導体装置に収納する半導体チップが厚くなり、半導体装置の薄形化ひいては機器の薄形化を阻害する要因となっている。さらに、半導体ウエハは裏面研削時のAuバンプへの荷重集中による半導体ウエハの破損を回避するために、Auバンプの形成を裏面研削後に行っているのが一般的であり、Auバンプを形成した後に裏面研削を行うことは、荷重の局部集中による半導体ウエハの破損を回避することを考慮すると、非常な困難さを伴うおそれがあった。

【0006】 一方、機器内の半導体装置が占める実装面積は、半導体素子の高集積化、高機能化にともない増大する方向にあり、特に、従来の半導体装置の内側はボンディングワイヤ、インナーリードなどの電気的導通経路を必要とし、かつ、半導体装置の外側には接合を得るためのアウターリードを必要とするために本質的に実装面積は大きくなり、さらには、樹脂厚みと半導体チップ厚みからなる実装高さも高くなり、これらのことが半導体装置の小型化、軽量化を阻害し、ひいては、機器の小型化、軽量化を阻害する要因となっていた。

【0007】 さらに、研削後に分割される半導体チップの素子面は外部からのわずかな力により簡単に損傷を受けやすく、組立工程や実装工程における半導体チップのハンドリングや装置条件の設定には細心の注意が必要であった。

【0008】 本発明は、半導体ウエハを裏面研削により薄く加工しても半導体ウエハ破損が生じないようにすることと同時に半導体チップの素子面への損傷が生じないようにすること、そして、2次元的な電気的導通経路を最小にして実装面積を小さくし、かつ、樹脂厚みおよび半導体チップ厚みを最小にして実装高さを小さくすることを目的としている。

## 【0009】

【課題を解決するための手段】 本発明の半導体装置は、前述のような課題を解決するものであって、その概要を説明すればつきの通りである。すなわち、外部接続端子となる突起電極を埋設した樹脂部を保護強化板としながら半導体ウエハ裏面部を研削して半導体ウエハを薄くし、この樹脂部から突起電極先端部および半導体ウエハのスクライブラインを露出させた後に樹脂部最表面の主部およびスクライブライン部表面に絶縁保護強化膜を形成してからスクライブラインを切断して半導体装置を構成させ、そして、この半導体装置上部の樹脂部の上面から突設された突起電極が外部接続端子として電気的かつ

機械的接合を得るように構成したものである。

【0010】

【作用】前述の手段によれば、半導体ウエハを裏面研削により薄く加工しても半導体ウエハ上に形成された樹脂部が保護強化板として機能するために、裏面研削中およびハンドリング時の半導体ウエハ破損を回避できるとともに、組立工程や実装工程におけるペア状態での半導体チップのハンドリングはなくなり、半導体チップの素子面への損傷も回避できる。また、半導体装置上部の樹脂部の大きさと半導体チップの大きさをほぼ同一となるようになり、前記半導体装置の上部に形成された樹脂部の上面から外部接続端子となる突起電極を突設することにより、容易に2次元的な電気的導通経路を最小にし、かつ、樹脂厚みおよび半導体チップ厚みを薄くさせた小型、薄型の半導体装置を形成することができる。

【0011】

【実施例】本発明の第1の実施例を図1および図2にもとづいて説明する。図1は本発明の第1の実施例の半導体装置を示す斜視図であり、図2は第1の実施例の半導体装置の製造方法について説明する断面図である。図1は表面に樹脂膜3および突起電極5を形成した半導体ウエハ1を個々の半導体チップ2の大きさに切断した状態を示しており、切断前において表面に樹脂膜3を形成した状態で半導体ウエハ1の裏面を裏面研削法を用いて鏡面状に研削を行って、半導体ウエハ1の厚みを薄く加工した後、スクライブライイン4をダイシングブレードを用いて切断している。この半導体ウエハ1の裏面の研削は、裏面研削前に半導体ウエハ1の表面に樹脂膜3を形成させることにより、樹脂膜3を保護強化板として機能させ、6インチ径の半導体ウエハ1であればウエハプロセス加工時の厚みが約0.6mmのものが裏面研削法により0.35mm～0.4mm程度まで半導体ウエハ1の厚みを薄く加工でき、8インチ径の半導体ウエハ1であってもウエハプロセス加工時の厚みが0.7mm程度のものが同様に0.4mm～0.5mm程度まで半導体ウエハ1の厚みを薄く加工できる。このことにより、半導体ウエハ1の厚み、すなわち、半導体ウエハ1の大きさ如何に関わらず半導体ウエハ1の厚みを薄く加工することができる。ここで、この樹脂膜3を形成する樹脂材料には、例えば低応力、高耐熱性を有するポリイミド樹脂を用いており、樹脂部の形成方法には一般によく用いられているポリイミド樹脂をスピンドルコートィングした後に熱硬化させる方法を用いている。また所定の樹脂膜厚を得るために、スピンドルコートィングを繰り返すことにより容易に得られる。なお、半導体ウエハ1の表面に形成される樹脂膜3の樹脂材料としては、前述のようなポリイミド樹脂の代わりに、低応力、低収縮性を有するエポキシ系の樹脂を用いることも可能であり、所定の樹脂膜3の厚みはスクリーン印刷法を用いることにより容易に得ることができ、この結果、樹脂膜3の保護強化板として

の機能はさらに向上することになる。

【0012】本発明の第1の実施例の半導体装置の製造方法を図2にもとづいて説明する。まず、第1の工程では図2Aに示すように、パターンが形成された0.6mm程度の厚みを有する半導体ウエハ1の電極パッド上に、クロム薄膜を介して電解メッキ法により選択的にAuメッキを施し、円柱状の突起電極5を約100μmの高さで形成する。つぎに、第2の工程では図2Bに示すように、半導体ウエハ1上に突起電極5の上端部を覆う程度の厚みで樹脂膜3を形成する。そして、第3の工程では図2Cに示すように、この樹脂膜3を保護強化板および接着剤として半導体ウエハ1の裏面を裏面研削法により研削し半導体ウエハ1の厚みを0.4mm程度となるよう薄く加工する。第4の工程では図2Dに示すように、半導体ウエハ1の上部に設けられた樹脂膜3の上面を軽くエッチングし、突起電極5の上端部を露出させる。第5の工程では図2Eに示すように、ダイシングブレードにてスクライブライイン4の樹脂膜3を削り取り、高温乾燥後、プラズマCVD法によりシリコンナイトライド膜6を突起電極5の上端部を除いて選択的に形成させる。最後に、第6の工程では図2Fに示すように、ダイシング用粘着性テープ(図示せず)にこの半導体ウエハ1を貼り、スクライブライイン4で半導体ウエハ1を完全にダイシングブレードにて削りとり、1個1個の半導体チップ2に分離する。なお、スクライブライイン4の樹脂膜3を取り除くためには、第5の工程で説明したような物理的な方法だけではなく、化学的エッチングによる方法も可能である。一方、シリコンナイトライド膜6の形成は、絶縁強化保護としての機能は若干低下するが、樹脂膜3の軽いエッチング直後に行うことも可能である。

【0013】さらに、図1において前述のように個々の半導体チップ2の大きさに切り出された半導体装置は、既に説明した通り裏面研削を施されて薄くなったり半導体チップ2の上面に樹脂膜3が形成されており、この樹脂膜3の上面からは半導体チップ2のパッド電極に対して垂直に形成された円柱状の突起電極5の先端部が突出しており、その突起電極5は電解メッキ法を用いて形成されたAu電極であり、その高さは80μm～100μmである。ただし、この突起電極5の形状は、円柱状であっても良いし、角柱状であっても良い。一方、この突起電極5の突出量は、突起電極5の高さ、樹脂膜3の厚み、そして、接合安定性から決定され、第1の実施例では20μm程度を突出させている。また、第1の実施例では、半導体チップ2の側面がダイシングされた状態で露出しており、同様にその裏面が研削された状態で露出している。さらに、図1では特に図示してはいないが、これら半導体チップ2の側面、裏面および突起電極5表面を除いた樹脂膜3最表面には半導体装置としての信頼性を高めるためのシリコンナイトライド膜6がプラズマ

CVD法により200°C~250°Cの比較的低温で1μm程度形成され、樹脂膜3への水分吸湿による半導体装置の信頼性低下を防ぐ絶縁強化保護膜としている。

【0014】本発明の第1の実施例の半導体装置を種々の実装形態に適合できることを示すプリント配線板への接合方法を図3にもとづいて説明する。図3は、図1に示した本発明の第1の実施例の半導体装置のプリント配線板への接合方法を示す断面図である。図3Aにしめすように、フットパターン8が形成されたプリント配線板7へ半導体装置が直接フェイスタウンボンディングされおり、フットパターン8上に予め設けられたAuバンプ9と半導体チップ2の突起電極5が熱圧着により合金接合されている。またこの合金接合部を含めた半導体装置の信頼性を高めるために、半導体装置の周縁部をエポキシ系の封止樹脂10をボッティング法で封止している。図3Bに示すように、図3Aに示した半導体装置の裏面に高熱伝導性のシリコン系接着剤11を塗布し、放熱板12となるAl合金板を貼付け、半導体装置からの放熱性を積極的に向上させている。図3Cは、半導体装置に形成された突起電極5のピッチが微細な場合についての実施例であり、通常のテープキャリア方式のTABテープと半導体チップ2との接合方法と全く同一な方法で、第1の実施例の半導体装置とTABテープ13とを突起電極5を介して接合させ、そして、このTABテープ13のリードの終端部とプリント配線板7上のフットパターン8とを半田接合法を用いて接合させ、この半田接合部を含む半導体装置の周縁部を図3A、図3Bと同様にエポキシ系の封止樹脂10でボッティング法により封止させた例である。図3Dは、図3Cで説明した半導体装置裏面に高熱伝導性のシリコン系接着剤11を塗布し、放熱板12となるAl合金板を貼り付け、半導体装置からの放熱性を向上させている。

【0015】次に、本発明の第2の実施例を図4にもとづいて説明する。図4Aは、本発明の第2の実施例の半導体装置を示す斜視図であり、図4Bは図4Aの側面図を示している。図4A、図4Bに示すように、裏面研削により薄く加工された半導体チップ2上に2つの異なる高さを有した突起電極5が千鳥状に半導体チップ2の周囲に形成されている。そして、半導体チップ2の内側に形成された突起電極5の配列には高い突起電極5が、その外側に形成された突起電極5の配列には低い突起電極5が形成され、突出量が20μm前後となるように樹脂膜3が段状に形成されている。このように半導体装置を構成したことにより、半導体チップ2上の突起電極5が微細ピッチとなっても、隣接リード間のショートが生じにくくTABボンディングが容易に行えるようになる。

【0016】つぎに本発明の第3の実施例および第4の実施例を、図5および図6にもとづいて説明する。図5および図6は、それぞれ第3の実施例および第4の実施例の半導体装置を示す斜視図である。図5に示す第3の

実施例は、半導体装置に突出させた突起電極5の周囲部の樹脂膜3に凹部14を形成させてあり、この凹部14を、図3Aに示す突起電極5とフットパターン8との接合材料にAuバンプ9の代わりに半田を用いたときに、隣接した突起電極5間での半田ブリッジによるショートを防ぐための半田だまりの役目を持たせている。一方、図6に示す第4の実施例は、半導体装置に突設させた突起電極5の上端部と円柱側部のうちの外側部を露出させた例であり、プリント配線板7に凹状の半導体装置収納部（図示せず）と前記半導体装置収納部の側面に縦状の導体パターン（図示せず）と底面に導体パターンを連続して設け、第4の実施例に示した半導体装置をプリント配線板7の半導体装置収納部に収納し、半導体装置の突起電極5の上端部と円柱側部とを前記導体パターンとを半田接合させるようにして半田接合時の信頼性向上をはかると同時に、プリント配線板7への実装時の高さの低減をはかっている。

【0017】以上説明してきたように、本発明の半導体装置は半導体チップ2の表面に樹脂膜3を形成することにより、半導体ウエハ1の破損、半導体チップ2の素子面の損傷を生じないようにすることができる。また、プリント配線板7への実装時の2次元的な電気導通経路を最小にすると同時に実装高さを小さくすることができる。

#### 【0018】

【発明の効果】本発明により得られる効果は、半導体ウエハを裏面研削により薄く加工しても半導体ウエハ上に形成された樹脂部が保護強化板として機能することにより裏面研削中およびハンドリング時の半導体ウエハ破損は回避できるようになったと同時に、組立工程や実装工程におけるペア状態の半導体チップのハンドリングがなくなり半導体チップの素子面への損傷も回避できるようになった。また、半導体装置上部の樹脂部の大きさと半導体チップの大きさをほぼ同一となるようにし、前記半導体装置上部の樹脂部の上面から外部接続端子となる突起電極を突設することにより、容易に、2次元的な電気的導通経路が最小で、かつ、樹脂厚みおよび半導体チップ厚みを薄くさせた高信頼性で小型かつ薄形の半導体装置を形成できるようになった。

#### 【図面の簡単な説明】

【図1】本発明の第1の実施例の半導体装置を示す斜視図。

【図2】本発明の第1の実施例の半導体装置の製造方法について説明する断面図。

【図3】本発明の第1の実施例の半導体装置のプリント配線板への接合方法を示す断面図。

【図4】本発明の第2の実施例の半導体装置を示す斜視図および断面図。

【図5】本発明の第3の実施例の半導体装置を示す斜視図。

【図6】本発明の第4の実施例の半導体装置を示す斜視図。

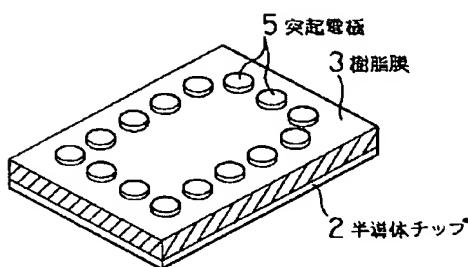
【図6】本発明の第4の実施例の半導体装置を示す斜視図である。

## 【符号の説明】

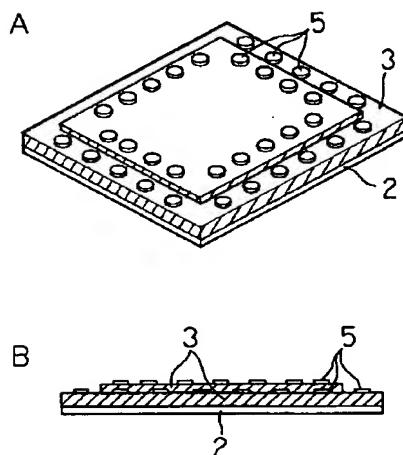
- 1 半導体ウエハ
- 2 半導体チップ
- 3 ポリイミド樹脂膜
- 4 スクライブライン
- 5 突起電極

- \* 6 シリコンナイトライド膜
- 7 プリント配線板
- 8 フットパターン
- 9 Auバンプ
- 10 封止樹脂
- 11 シリコン系接着剤
- 12 放熱板
- \* 13 TABテープ

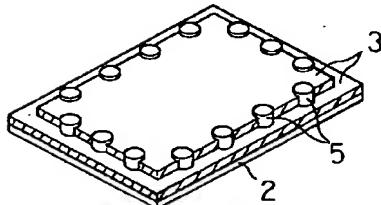
【図1】



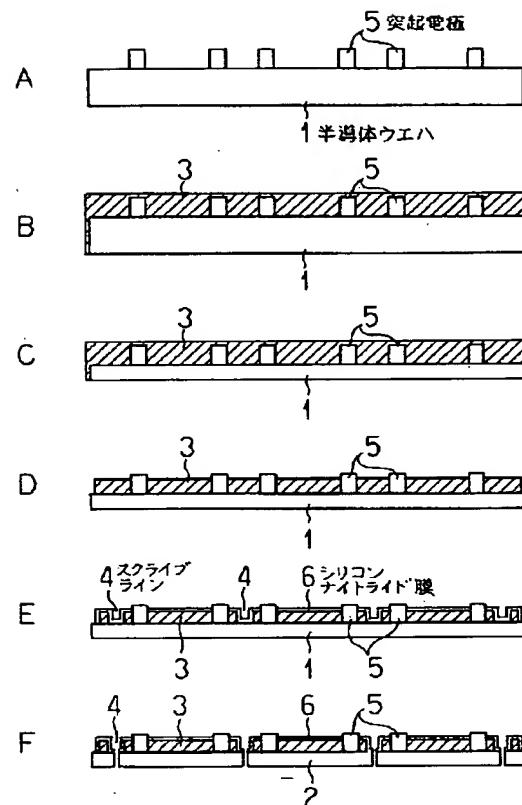
【図4】



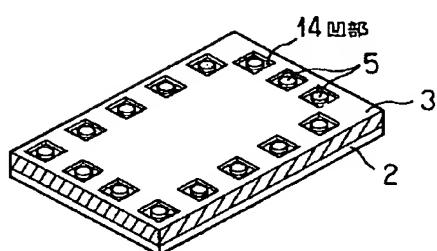
【図6】



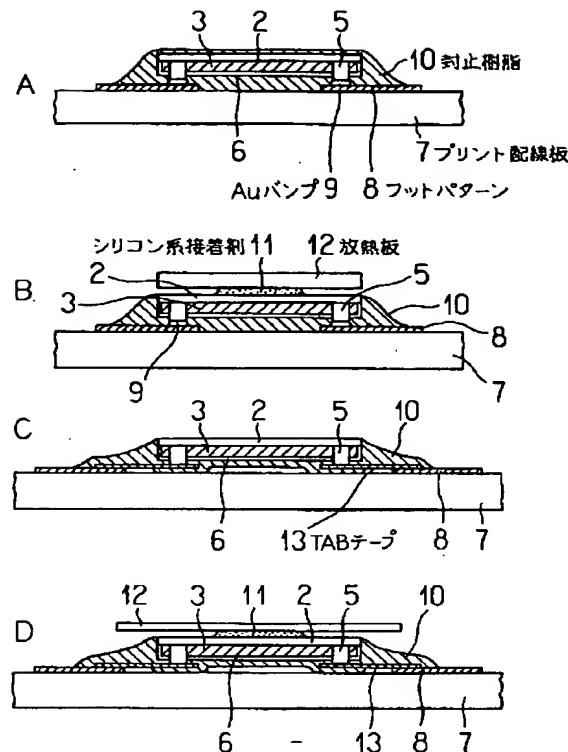
【図2】



【図5】



【図3】



フロントページの続き

(51) Int.Cl.<sup>3</sup>  
H 01 L 21/321  
23/12  
23/28

識別記号 序内整理番号 F 1  
A 8617-4M

技術表示箇所

## PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-055278  
 (43)Date of publication of application : 05.03.1993

(51)Int.Cl. H01L 21/56  
 H01L 21/304  
 H01L 21/78  
 H01L 21/321  
 H01L 23/12  
 H01L 23/28

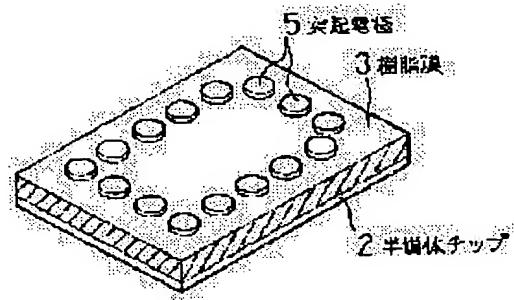
(21)Application number : 03-211207 (71)Applicant : SONY CORP  
 (22)Date of filing : 23.08.1991 (72)Inventor : NISHINO TOMONORI

## (54) SEMICONDUCTOR DEVICE

## (57)Abstract:

PURPOSE: To improve handling operability of a semiconductor chip in a manufacturing step while reducing in thickness of the chip itself irrespective of the size of a semiconductor wafer and to obtain a small-sized thin semiconductor device.

CONSTITUTION: A semiconductor wafer 1 is reduced in thickness while forming a resin film 3 in a protective reinforcing plate, protrusion electrodes 5 protrude from the film 3 on a semiconductor chip 2 as an external connection terminal, and the film 3 is so cut as to be the same in size as the chip 2. Thus, a semiconductor device having high reliability, easy handling, small size and thickness, is obtained.



## LEGAL STATUS

[Date of request for examination] 19.08.1998  
 [Date of sending the examiner's decision of rejection] 25.04.2000  
 [Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]  
 [Date of final disposal for application]  
 [Patent number] 3128878  
 [Date of registration] 17.11.2000  
 [Number of appeal against examiner's decision of rejection] 2000-07655  
 [Date of requesting appeal against examiner's decision of rejection] 23.05.2000  
 [Date of extinction of right]

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CLAIMS

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## [Claim(s)]

[Claim 1] The semiconductor device characterized by the side face and underside of a semiconductor chip being exposed, the resin section which has the almost same magnitude as this being formed in said semiconductor chip top face, and the projection electrode protruding from the top face of said resin section.

[Claim 2] A semiconductor device given in the application-for-patent term 1 characterized by forming the insulation protection consolidation film in the principal piece of the outermost surface of said resin section.

[Claim 3] The manufacture approach of a semiconductor device given in the application-for-patent term 1 characterized by making the semi-conductor wafer rear-face section remove, using as a protection consolidation plate the resin section under which said projection electrode was laid.

[Claim 4] The manufacture approach of a semiconductor device given in the application-for-patent term 1 characterized by forming the insulation protection consolidation film in the resin section outermost surface and a cutting field front face, and cutting a cutting field after exposing the cutting field of a projection electrode point and a semi-conductor wafer from said resin section.

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DETAILED DESCRIPTION

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## [Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the semiconductor device which makes the projection electrode point formed on the pad electrode layer of a semiconductor chip with an external connection terminal.

[0002]

[Description of the Prior Art] Grinding of the semi-conductor wafer which pattern formation generally completed is carried out to predetermined thickness using a rear-face grinding method. This rear-face grinding method is grinding and a thing to remove about a semi-conductor wafer rear face by \*\*\*\* by which \*\* ON of the diamond grain was carried out into resin, pressurizing homogeneity and rotating [ stick on the pattern side of a semi-conductor wafer the elasticity nature film which uses the vinyl chloride used as a protection film etc. as a base material, ] a semi-conductor wafer from on an elasticity film.

[0003] And the thing of cutting the scribe line of the semi-conductor wafer by which grinding was carried out, having divided into each semiconductor chip, having joined a semiconductor chip and an external terminal lead mutually electrically through a bonding wire or a TAB lead, and carrying out processing formation of the external terminal lead after a resin seal was a general technique.

[0004] Moreover, before carrying out grinding of the semi-conductor wafer rear face by said rear-face grinding method and removing it, barrier metal membranes, such as Cr, were formed in behind, and Au bump was made to form in it selectively with Au electrolysis plating, in order to make projection electrodes, such as Au bump, form on a semi-conductor wafer.

[0005]

[Problem(s) to be Solved by the Invention] The semiconductor device is carried in all devices, such as a computer, a workstation, a personal computer, a word processor, a cellular phone, and a small pocket camcorder, so much. In recent years, progress of the miniaturization of these devices and lightweight-izing is remarkable, and since the miniaturization of these devices, lightweight-izing and high-performance-izing, and advanced features progress further, the demand to the miniaturization of the semiconductor device carried in these devices, the formation of a thin form, and high-reliability-izing will be predicted to be what increases at an increasing tempo together with a demand called high integration of a semiconductor device, and advanced features from now on. However, with progress of diameter[ of macrostomia ]-izing of a semi-conductor wafer, the semiconductor chip which a limitation produces to make thickness thin by constraint called breakage prevention of the semi-conductor wafer at the time of handling or grinding, consequently is contained to a semiconductor device becomes thick, and thin form-ized \*\*\*\* of a semiconductor device has become the factor which checks thin form-ization of a device at processing of the semi-conductor wafer thickness by the conventional rear-face grinding method. Furthermore, as for the semi-conductor wafer, it was common to have formed Au bump after rear-face grinding, in order to avoid breakage of the semi-conductor wafer by the load concentration to Au bump at the time of rear-face grinding, and performing rear-face grinding, after forming Au bump had a possibility that it might be accompanied by extraordinary difficulty, when it took into consideration avoiding breakage of the semi-conductor wafer by local concentration of a load.

[0006] On the other hand, the component-side product which the semiconductor device within a device occupies It tends to increase with high integration of a semiconductor device, and advanced features. Especially The inside of the conventional semiconductor device needs electric flow paths, such as a bonding wire and an inner lead. A component-side product becomes large intrinsically [ since the outer lead for acquiring junction is needed for the outside of a semiconductor device ]. And further It had become the factor which the mounting height which consists of resin thickness and semiconductor chip thickness also becomes high, and these things check the miniaturization of a semiconductor device, and lightweight-ization, as a result checks the miniaturization of a device, and lightweight-ization.

[0007] Furthermore, the component side of the semiconductor chip divided after grinding tended to receive breakage simply according to few force from the outside, and needed careful caution for the handling of a semiconductor chip and setting out of equipment conditions in an erector degree or a mounting process.

[0008] This invention aims at making to make it the breakage to the component side of a semiconductor chip not arise in making it semi-conductor wafer breakage not arise, even if it processes a semi-conductor wafer thinly by rear-face grinding, and coincidence, and a two-dimensional electric flow path into min, and making a component-side product small, and making resin thickness and semiconductor chip thickness into min, and making mounting height small.

## [0009]

[Means for Solving the Problem] If the semiconductor device of this invention solves the above technical problems and the outline is explained, it will be as follows. Namely, using as a protection consolidation plate the resin section which laid the projection electrode used as an external connection terminal underground, carry out grinding of the semi-conductor wafer rear-face section, and a semi-conductor wafer is made thin. After exposing the scribe line of a projection electrode point and a semi-conductor wafer from this resin section and forming the insulation protection consolidation film in the principal piece of the resin section outermost surface, and a scribe line section front face, cut a scribe line and a semiconductor device is made to constitute. It constitutes so that junction electric [ the projection electrode which protruded from the top face of the resin section of this semiconductor device upper part ] as an external connection terminal, and mechanical may be acquired.

## [0010]

[Function] Even if it process a semi-conductor wafer thinly by rear face grinding, in order that the resin section formed on the semi-conductor wafer may function as a protection consolidation plate according to the above-mentioned means, while the semi-conductor wafer breakage at the time among rear face grinding of handling be avoidable, handling of the semiconductor chip in the raise in basic wages condition in an erector degree or a mounting process be lose, and can also avoid the breakage to the component side of a semiconductor chip. moreover, small [ which the two-dimensional electric flow path be easily made / small / into min, and made thin resin thickness and semiconductor chip thickness ], and a thin semiconductor device can be form by protrude the projection electrode which the magnitude of the resin section of the semiconductor device upper part and the magnitude of a semiconductor chip be make to become almost the same, and serve as an external connection terminal from the top face of the resin section formed in the upper part of said semiconductor device.

## [0011]

[Example] The 1st example of this invention is explained based on drawing 1 and drawing 2. Drawing 1 is the perspective view showing the semiconductor device of the 1st example of this invention, and drawing 2 is a sectional view explaining the manufacture approach of the semiconductor device of the 1st example. After drawing 1 shows the condition of having cut the semi-conductor wafer 1 in which the resin film 3 and the projection electrode 5 were formed on the front face, in the magnitude of each semiconductor chip 2, it performs grinding for the rear face of the semi-conductor wafer 1 in the shape of a mirror plane using a rear-face grinding method where the resin film 3 is formed in a front face before cutting, and it processes the thickness of the semi-conductor wafer 1 thinly, it is cutting the scribe line 4 using a dicing blade. The grinding of the rear face of this semi-conductor wafer 1 by making the resin film 3 form on the front face of the semi-conductor wafer 1 before rear-face grinding The resin film 3 is operated as a protection consolidation plate, and that whose thickness at the time of wafer process processing is about 0.6mm if it is the semi-conductor wafer 1 of the diameter of 6 inch can process the thickness of the semi-conductor wafer 1 thinly to 0.35mm - about 0.4mm by the rear-face grinding method. Even if it is the semi-conductor wafer 1 of the diameter of 8 inch, that whose thickness at the time of wafer process processing is about 0.7mm can process the thickness of the semi-conductor wafer 1 thinly to 0.4mm - about 0.5mm similarly. It can \*\*, if it is not concerned in the thickness of the semi-conductor wafer 1, i.e., the size of the semi-conductor wafer 1, how but the thickness of the semi-conductor wafer 1 is thinly processed by this. Here, after carrying out spin coating of the polyimide resin which uses the polyimide resin which has for example, low stress and high thermal resistance for the resin ingredient which forms this resin film 3, and is generally well used for the formation approach of the resin section, the approach of carrying out heat curing is used. Moreover, in order to obtain predetermined resin thickness, it is easily obtained by repeating spin coating. In addition, it will also be possible to use the resin of the epoxy system which has low stress and low shrinkage characteristics instead of the above polyimide resin as a resin ingredient of the resin film 3 formed in the front face of the semi-conductor wafer 1, and the thickness of the predetermined resin film 3 can be easily obtained by using squeegee print processes. consequently the function as a protection consolidation plate of the resin film 3 will improve further.

[0012] The manufacture approach of the semiconductor device of the 1st example of this invention is explained based on drawing 2. First, in the 1st process, as shown in drawing 2 A, on the electrode pad of the semi-conductor wafer 1 which has the thickness which is about 0.6mm in which the pattern was formed, Au plating is selectively performed with electrolysis plating through a chromium thin film, and the cylinder-like projection electrode 5 is formed in height of about 100 micrometers. Next, in the 2nd process, as shown in drawing 2 B, the resin film 3 is formed for the upper bed section of the projection electrode 5 by the thickness of wrap extent on the semi-conductor wafer 1. And at the 3rd process, as shown in drawing 2 C, grinding of the rear face of the semi-conductor wafer 1 is carried out by the rear-face grinding method by using this resin film 3 as a protection consolidation plate and adhesives, and the thickness of the semi-conductor wafer 1 is thinly processed so that it may be set to about 0.4mm. At the 4th process, as shown in drawing 2 D, the top face of the resin film 3 established in the upper part of the semi-conductor wafer 1 is etched lightly, and the upper bed section of the projection electrode 5 is exposed. The resin film 3 of the scribe line 4 is shaved off with a dicing blade, and the silicon nitride film 6 is made to form selectively except for the upper bed section of the projection electrode 5 after elevated-temperature desiccation by the plasma-CVD method at the 5th process, as shown in drawing 2 E. Finally, at the 6th process, as shown in drawing 2 F, this semi-conductor wafer 1 is stuck on the adhesive tape for dicing (not shown), the semi-conductor wafer 1 is thoroughly shaved off with a dicing blade in the scribe line 4, and it separates into the one-piece one semiconductor chip 2. In addition, in order to remove the resin film 3 of the scribe line 4, not only a physical approach that was explained at the 5th process but the approach by chemical etching is possible. On the other

hand, formation of the silicon nitride film 6 can also be carried out immediately after light etching of the resin film 3, although the function as insulating consolidation protection falls a little.

[0013] Furthermore, the semiconductor device cut down by the magnitude of each semiconductor chip 2 as mentioned above in drawing 1 The resin film 3 is formed in the top face of the semiconductor chip 2 which rear-face grinding was given and became thin as already explained. From the top face of this resin film 3, the point of the projection electrode 5 of the shape of a cylinder vertically formed to the pad electrode of a semiconductor chip 2 projects, that projection electrode 5 is an Au electrode formed using electrolysis plating, and that height is 80 micrometers – 100 micrometers. However, the configuration of this projection electrode 5 may be cylindrical, and may be a prismatic form. On the other hand, the amount of projection of this projection electrode 5 is determined from the height of the projection electrode 5, the thickness of the resin film 3, and junction stability, and is making about 20 micrometers project in the 1st example. Moreover, in the 1st example, it has exposed, where the dicing of the side face of a semiconductor chip 2 is carried out, and where grinding of the rear face is carried out similarly, it has exposed. Furthermore, although not illustrated especially in drawing 1, the silicon nitride film 6 for raising the dependability as a semiconductor device to the resin film 3 outermost surface except the side face of these semiconductor chips 2, a rear face, and projection electrode 5 front face is considering as the insulating consolidation protective coat which prevents the dependability lowering of the semiconductor device about 1 micrometer is comparatively formed at low temperature, and according to the moisture moisture absorption to the resin film 3 of 200 degrees C – 250 degrees C by the plasma-CVD method.

[0014] The junction approach to the printed wired board which shows that various mounting gestalten can be suited in the semiconductor device of the 1st example of this invention is explained based on drawing 3. Drawing 3 is the sectional view showing the junction approach to the printed wired board of the semiconductor device of the 1st example of this invention shown in drawing 1. Direct face down bonding of the semiconductor device is carried out to the printed wired board 7 in which the foot pattern 8 was formed, and alloy junction of the projection electrode 5 of the Au bump 9 and semiconductor chip 2 which were beforehand prepared on the foot pattern 8 is carried out by thermocompression bonding so that it may be shown in drawing 3 A. Moreover, in order to raise the dependability of a semiconductor device including this alloy junction section, the closure resin 10 of an epoxy system is closed for the periphery section of a semiconductor device by the potting method. As shown in drawing 3 B, the silicon system adhesives 11 of high temperature conductivity are applied to the rear face of the semiconductor device shown in drawing 3 A, aluminum alloy plate used as a heat sink 12 is stuck, and the heat dissipation nature from a semiconductor device is raised positively. Drawing 3 C is the example of an about when the pitch of the projection electrode 5 formed in the semiconductor device is detailed, and it is the completely same approach as the junction approach of the TAB tape of the usual tape career method, and a semiconductor chip 2. The 1st semiconductor device and TAB tape 13 of an example are joined through the projection electrode 5. It is the example which made the periphery section of the semiconductor device which is made to join the trailer of a lead of this TAB tape 13, and the foot pattern 8 on a printed wired board 7 using the joining method, and contains this soldered joint section close by the potting method by the closure resin 10 of an epoxy system like drawing 3 A and drawing 3 B. Drawing 3 D applies the silicon system adhesives 11 of high temperature conductivity to the semiconductor device rear face explained by drawing 3 C, sticks aluminum alloy plate used as a heat sink 12, and is raising the heat dissipation nature from a semiconductor device.

[0015] Next, the 2nd example of this invention is explained based on drawing 4. Drawing 4 A is the perspective view showing the semiconductor device of the 2nd example of this invention, and drawing 4 B shows the side elevation of drawing 4 A. As shown in drawing 4 A and drawing 4 B, the projection electrode 5 with two different height is alternately formed around the semiconductor chip 2 on the semiconductor chip 2 thinly processed by rear-face grinding. And the projection electrode 5 with the high projection electrode 5 low in the array of the projection electrode 5 formed in the outside is formed in the array of the projection electrode 5 formed inside the semiconductor chip 2, and the resin film 3 is formed in the shape of a stage so that the amount of projection may become 20-micrometer order. Thus, even if the projection electrode 5 on a semiconductor chip 2 serves as a detailed pitch by having constituted the semiconductor device, TAB bonding which the short circuit during a contiguity lead cannot produce easily can be performed easily.

[0016] The 3rd example and 4th example of this invention are explained based on drawing 5 and drawing 6 below. Drawing 5 and drawing 6 are the perspective views showing the semiconductor device of the 3rd example and the 4th example, respectively. the 3rd example show in drawing 5 be the solder for preventing the short circuit by the solder bridge between the adjoining projection electrodes 5, when solder use for the cementing material of the projection electrode 5 and the foot pattern 8 which be make to have form the crevice 14 in the resin film 3 of the perimeter section of the projection electrode 5 which made the semiconductor device project, and show this crevice 14 to drawing 3 A instead of an Au bump 9 — the duty of a ball be giving. On the other hand, the 4th example shown in drawing 6 is an example for which the upper bed section of the projection electrode 5 made to protrude on a semiconductor device and the lateral part of the cylinder flanks were exposed. A conductor pattern is continued and prepared in the side face of a concave semiconductor device stowage (not shown) and said semiconductor device stowage on length-like a conductor pattern (not shown) and a base at a printed wired board 7. The semiconductor device shown in the 4th example is contained to the semiconductor device stowage of a printed wired board 7. Reduction of the height at the time of mounting to a printed wired board 7 is aimed at at the same time it aims at the improvement in dependability at the time of a soldered joint, as said conductor pattern is joined with solder for the upper bed section and the cylinder flank of the projection electrode 5 of a semiconductor

device.

[0017] The semiconductor device of this invention can be prevented from producing breakage of the semi-conductor wafer 1, and breakage on the component side of a semiconductor chip 2 by forming the resin film 3 in the front face of a semiconductor chip 2, as explained above. Moreover, mounting height can be made small while making the two-dimensional electric flow path at the time of mounting to a printed wired board 7 into min.

[0018]

[Effect of the Invention] Even if the effectiveness acquire by this invention processed the semi-conductor wafer thinly by rear face grinding, when the resin section formed on the semi-conductor wafer functioned as a protection consolidation plate, while the semi-conductor wafer breakage at the time among rear face grinding of handling could be avoided, handling of the semiconductor chip of the raise in basic wages condition in an erector degree or a mounting process is lose, and the breakage to the component side of a semiconductor chip could also be avoided. moreover, the semiconductor device of small and a thin form can be form now with the high-reliability which a two-dimensional electric flow path be [ high-reliability ] min, and made thin easily resin thickness and semiconductor chip thickness by protrude the projection electrode which the magnitude of the resin section of the semiconductor device upper part and the magnitude of a semiconductor chip be make to become almost the same, and serve as an external connection terminal from the top face of the resin section of said semiconductor device upper part.

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DESCRIPTION OF DRAWINGS

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## [Brief Description of the Drawings]

[Drawing 1] The perspective view showing the semiconductor device of the 1st example of this invention.

[Drawing 2] The sectional view explaining the manufacture approach of the semiconductor device of the 1st example of this invention.

[Drawing 3] The sectional view showing the junction approach to the printed wired board of the semiconductor device of the 1st example of this invention.

[Drawing 4] The perspective view and sectional view showing the semiconductor device of the 2nd example of this invention.

[Drawing 5] The perspective view showing the semiconductor device of the 3rd example of this invention.

[Drawing 6] It is the perspective view showing the semiconductor device of the 4th example of this invention.

## [Description of Notations]

1 Semiconductor Wafer

2 Semiconductor Chip

3 Polyimide Resin Film

4 Scribe Line

5 Projection Electrode

6 Silicon Nitride Film

7 Printed Wired Board

8 Foot Pattern

9 Au Bump

10 Closure Resin

11 Silicon System Adhesives

12 Heat Sink

13 TAB Tape

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